Accellera IP Tagging Standard Frequently Asked Questions

1. What is IP-Tagging

IP Tagging provides a way to track IP information as it passes throughout the design and development process. The design process can include editing, synthesis, timing, placement, wiring, and other steps leading to GDSII generation. Semiconductor foundries, providers of IP blocks, and design tool providers can use the methods described by an IP tagging standard to track identification information throughout each level of the development process and more specifically, in the final GDSII database.

2. What is the current state of art

Tags are intended to be readable on the text layer of the GDS format and previous IP Tagging implementations have been specific to cells and hard IP. Hard IP tags are widely used by developers and users of library, memory and Hard IP, such as technology specific PHYs, as well as foundries who track the use of silicon intellectual property (IP) in chips manufactured in their fabs. However, text tags instantiated in soft IP have not been recognized or carried forward by traditional EDA tools and are therefore not currently available in the GDSII database to verify actual implementation and usage

3. What is the expected "additional contribution" from Accellera

The Accellera technical subcommittee will update the existing soft IP tagging standard to align with the hard IP tagging approach currently in wide use. The soft IP Tagging structure and requirements will be documented in a normative standard. A corresponding white paper will be developed to illustrate an implementation approach that is independent of any changes to existing EDA tools. Additional topics for FPGA and ESL applications may also be addressed.

4. What additional benefits do we get as a result of this contribution

IP tagging enables a data-driven methodology to track the IP usage in an SoC's GDSII. Extending the tagging capability to soft IP provides a means to track all IP, not just the hardened IPs, for royalty calculations or other contractual IP usage obligations, as well as "where used" instantiated version linkage for bugs and errata among other tracking applications.

5. When can I expect to see this new standard released

As with any volunteer development effort, the final schedule is at the mercy of the participant's day jobs, however we hope to have something released in 2012.

6. Where can I find additional info on this effort

Read the press release at http://www.accellera.org/news/2011/Accellera_IP_Tagging_042611-3.pdf. Accellera members can subscribe to the group at http://www.accellera.org/apps/org/workgroup/tagging and non-members should contact Accellera at http://www.accellera.org/contact_us. The group is interested in hearing about additional issues in tracking IP or other use models for IP tracking.